

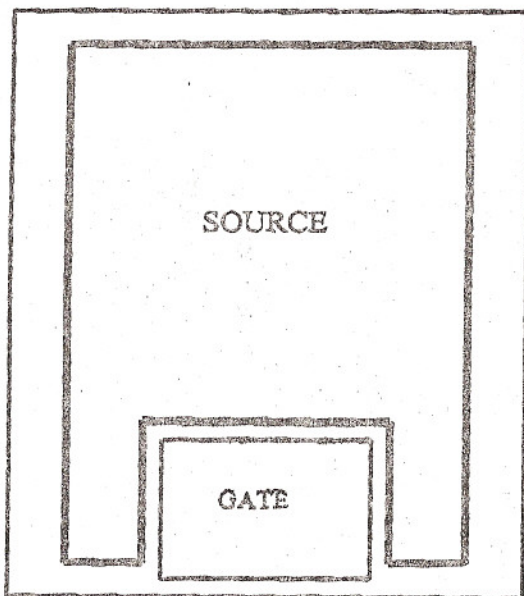


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Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below.

HEX-1: -100V, P- CHANNEL, GEN 5
MANF DRAWING NO.:- 01-5223



GATEPAD: 20 X 25 MILS

Topside Metal: Aluminum
Backside: CrNiAg
Backside Potential: Drain
Mask Ref: GEN V
Bond Pads (Mils): See Above

APPROVED BY:
MFG: Linear Sytems

DIE SIZE: .069" X .091"
THICKNESS: .014"

DATE: 10/1/99
P/N: IRFC9120NB

DG 10.1.2
Rev A 3-4-99

FAXED